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10/804,024	03/19/2004	Charles Douglas Murphy		6929

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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/804,024	MURPHY, CHARLES DOUGLAS
	Examiner	Art Unit
	James Cho	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5 and 7-20* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed October 4, 2004.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "means for allowing said first sensor output to change in response to incident energy" recited in claim 19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19, "means for allowing said first sensor output to change in response to incident energy" appears to be the function of "a first sensor" as described on lines 14-19 on page 9 of the specification instead of a separate and distinctive means.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-5 and 7-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Laflaquiere et al. (US PAT No. 6,850,176).

Regarding claim 2, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system comprising: a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) having a first sensor output (output applied to node 35), a threshold detector

(comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node β), the threshold detector comprising: a first transistor (34) having a first gate the first transistor being an n-type MOS transistor (34 is NMOS denoted by the arrow pointing outward), a second transistor (33) having a second gate, the second transistor being a p-type MOS transistor (32 is PMOS denoted by the arrow pointing inward), means for applying the first analog input to the first gate and to the second gate (input node 35 is coupled to gates of 33 and 34 via 31 and 32), and means for applying the first sensor output as the first analog input (conductor carrying the output signal from the sensor 20,30,22,24, to the node 35).

Regarding claim 3, Fig. 6 of Laflaquiere et al. teaches the machine of claim 2 in which the first transistor has a first transistor drain and a first transistor source, the second transistor has a second transistor drain and a second transistor source, the first transistor drain and the second transistor source are directly connected (33 and 34 having drain and source respectively are directly coupled in series where the drain of 34 is coupled to the source of 33).

Regarding claim 4, Fig. 6 of Laflaquiere et al. teaches the machine of claim 3 in which the first transistor source is directly connected to a first power supply rail (ground) the second transistor drain is directly connected to a second power supply rail (Vr).

Regarding claim 5, Fig. 6 of Laflaquiere et al. teaches the machine of claim 4 in which the first power supply rail has a more negative potential than the second power supply rail (ground is more negative than Vr).

Regarding claim 7, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) having a first sensor output (output applied to node 35), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node β), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first sensor output as the first analog input (conductor carrying the output signal from the sensor 20,30,22,24, to the node 35), and the threshold detector comprising an inverter (26 has an inverter comprising of transistors 33 and 34).

Regarding claim 8, Fig. 6 of Laflaquiere et al. teaches the machine of claim 7 in which the inverter comprises the first transistor (33) and the second transistor (34).

Regarding claim 9, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) having a first sensor output (output applied to node 35), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node β), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first sensor output as the first analog input (conductor carrying the output signal from the sensor 20,30,22,24, to the node 35), and the threshold detector comprising a digital logic circuit (transistors 33 and 34 forms an inverter digital logic gate).

Regarding claim 10, Fig. 6 of Laflaquiere et al. teaches the machine of claim 9 in which the digital logic gate comprises the first transistor (33) and the second transistor (34).

Regarding claim 11, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) having a first sensor output (output applied to node 35), a threshold detector

(comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node β), the threshold detector being a single-input threshold detector with an implicit threshold level (non-external and implicit threshold voltage defined by intrinsic characteristics of transistors forming the comparator; col. 5, lines 20-23), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first sensor output as the first analog input (conductor carrying the output signal from the sensor 20,30,22,24, to the node 35).

Regarding claim 12, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) having a first sensor output (output applied to node 35), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node β), the threshold detector comprising: a first transistor (34) having a first gate, a second transistor (33) having a second gate, means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first sensor output as the first analog input (conductor carrying the output signal from the sensor 20,30,22,24, to

the node 35), in the machine the first transistor and the second transistor being located substantially adjacent to the first sensor (Fig. 6 is an exemplary PEL, a digital elementary input, located in a column; col. 4, lines 7-14 where the sensor, 20,30,22,24, is substantially adjacent to 33 and 34 through 33 and 34 and there is no long wires required between as shown in Fig. 6 but coupled to transistors via 31 and 32) whereby long wires connecting the first sensor, the first transistor, and the second transistor are not required.

Regarding claim 13, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) having a first sensor output (output applied to node 35), a threshold detector (comparator 26 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) having a first analog input (input coupled to node 35) and a first digital output (output at node β), the threshold detector comprising: a first transistor (34) having a first gate, the first transistor being a minimum-size transistor (34 is minimum-sized compared to a big sized power transistor), a second transistor (33) having a second gate, the second transistor being a minimum-size transistor (33 is minimum-sized compared to a big sized power transistor), means for applying the first analog input to the first gate and to the second gate (signal at node 35 is applied to the gates of 33 and 34 via 31 and 32), and means for applying the first sensor output as the first analog input (conductor carrying the output signal from the sensor 20,30,22,24, to the node 35)

whereby the semiconductor chip area occupied by the first transistor and the second transistor is less than would be required for non-minimum-size transistors (it's inherent that the smaller first and second transistors would occupy less chip area compared to bigger sized first and second transistors).

Regarding claim 14, Fig. 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a multiplicity of threshold detectors (multiple PELs of Fig. 6 are connected in rows and columns by buses; col. 4, lines 7-20 where each of PELs has a comparator 26 functioning as a threshold detector), each having an input line connected to the gates of at least two transistors (each detector 26 has two transistors 33 and 34 whose gates are coupled to the input node 35 via 31, 32), a digital output (output at node β), a multiplicity of sensors (sensor comprising photo-detector 20, switch 30, integrator 22, reset device 24) each having a sensor output (output applied to node 35) provided as input to the input line of one of the multiplicity of threshold detectors (node 35 is coupled to the output of sensor as well as input of the detector 26), means for measuring a multiplicity of elapsed times when the digital outputs of the threshold detectors change states (determining the time period between the start of the integration time and the instant when the threshold value is exceeded as shown in Fig. 5 and stated in col. 3, lines 52-64, col. 4, lines 54-58, col. 6, lines 37-42 inherently requires a means for measuring the time elapsed).

Regarding claim 15. Fig. 6 of Laflaquiere et al. teaches the machine of claim 14 in which the threshold detectors are single-input threshold detectors with implicit thresholds (non-external and implicit threshold voltage defined by intrinsic characteristics of transistors forming the comparator; col. 5, lines 20-23).

Regarding claim 16. Fig. 6 of Laflaquiere et al. teaches the machine of claim 14 in which the threshold detectors are digital logic gates (26 has a digital logic inverter comprising transistors 33 and 34).

Regarding claim 17. Fig. 6 of Laflaquiere et al. teaches the machine of claim 14 in which the threshold detectors are inverters (26 has a digital logic inverter comprising transistors 33 and 34).

Regarding claim 18. Fig. 6 of Laflaquiere et al. teaches the machine of claim 17 in which the inverters consist of minimum-size transistors (transistors 33 and 34 are minimum-sized compared to a big sized power transistor),

Regarding claim 19, Figs. 3 and 6 of Laflaquiere et al. teaches a machine for time-to-threshold analog-to-digital conversion in a digital imaging system, comprising: a. a first sensor (sensor comprising photo-detector 20, switch 30, integrator 22 in Fig. 6) providing a first sensor output (output applied to node 35 in Fig. 6), means for initializing the first sensor output to a first sensor output level (reset transistor 24 in Fig. 6; col. 5,

lines 51-60), means for allowing the first sensor output to change in response to incident energy (sensor output at node 35 is being changed based on the incident wave at photo-detector 20 via coupling transistor 30 and integrator 22), a first digital counter providing a digital elapsed time count (converter 19 in Fig. 3 performs counting 0s and 1s and provides digital values; col. 5, lines 41-44), means for detecting when the first sensor output reaches a first threshold level (comparator 26 in Fig. 6 detects an input voltage and compared with a threshold voltage; col. 5, lines 23-35) comprising a first transistor (33 in Fig. 6) having a first gate, a second transistor (34 in Fig. 6) having a second gate, a digital indicator output signal for indicating when the first sensor output reaches the first threshold level (output at node β), means for applying the first sensor output to the first gate (conductor connecting the node 35 to the gate of 33 through 31 and 32), means for applying the first sensor output to the second gate (conductor connecting the node 35 to the gate of 34 through 31 and 32), means for recording a first value of the digital elapsed time count on the basis of a change in the digital indicator output signal (digital values are stored in a memory; col. 7, lines 38-40).

Regarding claim 20, Figs. 3 and 6 of Laflaquiere et al. teaches the machine of claim 19 in which the means for detecting when the first sensor output reaches the first threshold level is an inverter (comparator 26 in Fig. 6 has an inverter comprising 33 and 34), and the digital indicator output signal is the digital output of the inverter (output at node β is the output of the inverter).

Response to Arguments

Applicant's arguments with respect to claims 2-20 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Laflaquiere et al. teaches an A/D converter with a photo-detection sensor, one of ordinary skill in the art would not have been motivated to modify the teaching of Laflaquiere et al. to further includes, among other things, the specific of the first power supply rail being more negative potential than the second power supply rail.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Terazawa et al. (US PAT No. 6,940,443) discloses an A/D converter with a pulse delay circuit having a logic circuit.

Yun et al. (US PAT No. 6,943,719) discloses an A/D converter for image sensor with an inverter circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on Monday-Thursday 5:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho

James H. Cho
Primary Examiner
Art Unit 2819

Date: 12-27-2005